ABSTRACT

Non-Volatile RAM Cell and Array using Nanotube Switch Position for Information State. A non-volatile memory array includes a plurality of memory cells, each cell receiving a bit line, word line, and release line. Each memory cell includes a cell selection transistor with first, second and third nodes. The first and second nodes are in respective electrical communication with the bit line and the word line. Each cell further includes an electromechanically deflectable switch, having a first, second and third node. The first node is in electrical communication with the release line, and a third node is in electrical communication with the third node of the cell selection transistor. The electromechanically deflectable switch includes a nanotube switching element physically positioned between the first and third nodes of the switch and in electrical communication with the second node of the switch. The second node of the switch is in communication with a reference signal. Each nanotube switching element is deflectable into contact with the third node of the switch in response to signals at the first and second node of the cell selection transistor and is releasable from such contact in response to a signal at the release line. In preferred embodiments, the cell selection transistor is a FET and the second node of the transistor is a gate of the FET.